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10/607,819	06/27/2003	Rajesh Kota	NWISP046	8385

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BEYER WEAVER LLP
P.O. BOX 70250
OAKLAND, CA 94612-0250

EXAMINER	
NASH, LASHANYA RENEE	
ART UNIT	PAPER NUMBER
2453	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/607,819	KOTA ET AL.	
	Examiner	Art Unit	
	LASHANYA R. NASH	2453	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 July 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *6/27/2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office action is in response to the amendments filed 30 July 2008. Claims 1-31 are presented for further consideration. Claims 1, 12, and 23 are currently amended.

Response to Arguments

Applicant's arguments, see Remarks, filed 30 July 2008, with respect to the rejections of claims 1-31 under 35 USC 103(a) have been fully considered and are persuasive in light of the amendments. Therefore, the rejection has been withdrawn. However, upon further consideration, a new grounds of rejection is made in view of a newly found prior art reference Barroso et al., as set forth below in the Office action.

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference signs mentioned in the description: 701, 711, 713, 715, 717, 719, 721 (pages 16-17). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner,

the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 7, 13, 18, 24 and 29 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 7, 18, and 29 recite the limitation "the polling". There is insufficient antecedent basis for this limitation in the claim. There is no mention of polling in the preceding claims, ad therefore a state associated with the polling has no antecedent basis and furthermore is confusing.

Claims 13 and 24 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01. The omitted steps are: polling for a link from the first interconnection controller to a second interconnection controller. With the omission of these steps, there is no distinction made regarding which elements the claimed polling is to be performed continuously between, thereby rendering the claims indefinite.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-2, 4-6, and 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Self et al. (US Patent 5,623,644) in view of Barroso et al. ["Piranha: A Scalable Architecture Based on Single-Chip Multiprocessing"- retrieved from IEEE], hereinafter referred to as Self and Barroso respectively.

In reference to claim 1, Self discloses a point-to-point communication apparatus (abstract). Self further discloses:

- A computer system (Figures 17-18), comprising:
- A first cluster (i.e. micro-cluster; Figure 18-item 1850; column 14, lines 1-14) including a first plurality of processors (Figure 18-items 1812-1813), and first interconnection controller (i.e. router/memory controller; Figure 18-item 1811), each of the plurality of processors has a point to point link to the first interconnection controller (Figure 18-arrow from processor 1812, 1813 to router 1811), (i.e. point-to-point interconnection; column 14, lines 3-19);
- A second cluster (Figure 18-item 1851) including a second plurality of processors (Figure 18-processors for cluster 1851) and a second

interconnection controller (Figure 18-router/memory controller), the second interconnection controller connected to the first interconnection controller (column 10, lines 35-52; column 14, lines 10-26).

However, the reference fails to disclose that the first and second clusters both include, a plurality of configuration registers, a plurality of memory banks, a service processor, and wherein each of the processors has a first point-to-point link to a corresponding memory bank, a second point-to-point link to the service processor; and wherein indicators in the first plurality of CSRs are toggled to disconnect the second interconnection controller from the first interconnection controller. Nonetheless, this would have been an obvious modification to the teachings of Self for one of ordinary skill in the art at the time of the invention, as further evidenced by Barroso.

In an analogous art, Barroso discloses a microprocessor system (abstract). Barroso further discloses a plurality of configuration registers (i.e. space registers for PCI; ***2 Piranha Architecture Overview***, paragraph 3, page 284), a plurality of memory banks (i.e. banks of RDRAM; Figure 1-direct rambus array), a service processor (i.e. system control; Figure1), and wherein each of the processors has a first point-to-point link to a corresponding memory bank, a second point-to-point link to the service processor (connections to processors, Figure 1-CPU), (***2 Piranha Architecture Overview***, paragraph 1, page 283); and wherein indicators in the first plurality of CSRs are toggled to disconnect the second interconnection controller from the first interconnection controller (i.e. interconnection system accesses registers for connection channel initialization; ***2.6 System Interconnect***, paragraph 2, page 287). One of

ordinary skill in the art would have been so motivated to accordingly modify the teachings of Self to further employ the architecture taught by Barroso so as to implement multiprocessors in a modular and scalable fashion (Barroso, ***1 Introduction***, paragraph 5, page 283).

In reference to claim 2, Self shows the first cluster of processors and the second clusters of processors share a single virtual address space (column 11, lines 46-column 12, line 8).

In reference to claim 4, Self shows wherein the first interconnection controller includes a fence indicator configurable to prevent the transmission of logical packets between the first interconnection controller and the second interconnection controller (column 14, lines 27-49).

In reference to claim 5, Self shows wherein the first interconnection controller includes a re-initialization indicator configurable to direct the first interconnection controller to reinitialize the link (column 8, lines 28-38; column 9, lines 15-27).

In reference to claim 6, Self shows wherein re-initialization comprises having a transmitter associated with the first interconnection controller send training sequence to the second interconnection controller (column 8, lines 28-38; column 9, lines 15-27).

In reference to claim 9, Self shows wherein re-initialization comprises having an associated with the first interconnection controller send an initialization sequence to the second interconnection controller (column 14, lines 10-26).

In reference to claim 10, Self shows wherein the first interconnection controller includes a plurality of cluster ID indicators operable to hold values identifying remote clusters of processors (column 14, lines 11-26).

In reference to claim 11, Self shows wherein the first interconnection controller includes, fence, re-initialization and cluster ID bits (column 11, lines 46-column 12, line 8; column 11, lines 46-column 12, line 8) and Booth shows configuration space registers comprising physical layer enable (column 13, lines 63-column 14, line 8).

Claims 12, 15-17, 20-23, 26-28 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Self et al. (US Patent 5,623,644) in view Barroso et al. ["Piranha: A Scalable Architecture Based on Single-Chip Multiprocessing"- retrieved from IEEE] and Sgroi et al. ["Addressing the System-on-a-chip Interconnection Woes Through Communication-Based Design" retrieved from ACM], hereinafter referred to as Self , Barroso and Sgroi respectively.

In reference to claim 12 and 23, Self discloses a point-to-point communication method and point-to-point apparatus communication (abstract), Self further discloses:

- Configuring a first interconnection controller (i.e. router/memory controller; Figure 18-item 1811) in a first cluster (i.e. micro-cluster; Figure 18-item 1850; column 14, lines 1-14) including a first plurality of processors (Figure 18-items 1812-1813), and, each of the plurality of processors has a point to point link to

the first interconnection controller (Figure 18-arrow from processor 1812, 1813 to router 1811), (i.e. point-to-point interconnection; column 14, lines 3-19);

- A second cluster (Figure 18-item 1851) including a second interconnection controller (Figure 18-router/memory controller) and a second plurality of processors (Figure 18-processors for cluster 1851) in communication using a point-to-point architecture (column 10, lines 35-52; column 14, lines 10-26).

However, the reference fails to disclose that the first and second clusters both include, a plurality of configuration registers, a plurality of memory banks, a service processor, and wherein each of the processors has a first point-to-point link to a corresponding memory bank, a second point-to-point link to the service processor; asserting a reset signal in a second interconnection controller. Nonetheless, this would have been an obvious modification to the teachings of Self for one of ordinary skill in the art at the time of the invention, as further evidenced by Barroso.

In an analogous art, Barroso discloses a microprocessor system (abstract). Barroso further discloses a plurality of configuration registers (i.e. space registers for PCI; ***2 Piranha Architecture Overview***, paragraph 3, page 284), a plurality of memory banks (i.e. banks of RDRAM; Figure 1-direct rambus array), a service processor (i.e. system control; Figure1), and wherein each of the processors has a first point-to-point link to a corresponding memory bank, a second point-to-point link to the service processor (connections to processors, Figure 1-CPU), (***2 Piranha Architecture Overview***, paragraph 1, page 283); and asserting a reset signal in a second interconnection controller (i.e. interconnection system initializes a reset; ***2.6***

System Interconnect, paragraph 2, page 287). One of ordinary skill in the art would have been so motivated to accordingly modify the teachings of Self to further employ the architecture taught by Barroso so as to implement multiprocessors in a modular and scalable fashion (Barroso, ***1 Introduction***, paragraph 5, page 283). However, the references fail to disclose enabling physical layer communications between the first and second interconnection controllers without enabling link layer communications between the first and second interconnection controllers, and after enabling the physical layer communication establishing a link layer protocol on a connection between the first and second interconnection controllers. Nonetheless, these features would have been obvious modifications to Self and Barroso for one of ordinary skill in the art at the time of the invention, as further evidenced by Sgroi.

In an analogous art, Sgroi discloses a communication based design of network-on-chip employing OSI layers model implementation (abstract). Sgroi further discloses enabling physical layer communications without enabling link layer communications (i.e. interface is actually the physical layer…no data-link layer is required; page 669, *An NOC Example:The Pleiades Platform*, paragraph 2) and after enabling the physical layer communication establishing a link layer protocol on a connection (page 670, *3.2. A Metropolis Example:Itercom*, paragraphs 3-5). One of ordinary skill in the art would have been so motivated to accordingly modify the communications between the first and second interconnection controllers so as to implement protocols of the OSI layers that match the needs of the system components (i.e. not necessary to implement all of the

OSI layers for high-functionality), (Sgroi page 669, *2. OSI Reference Model Applied to NOCs*, paragraph 9).

In reference to claims 15 and 26, Self shows wherein the first interconnection controller includes a fence indicator configurable to prevent the transmission of logical packets between the first interconnection controller and the second interconnection controller (column 14, lines 27-49).

In reference to claim s 16 and 27, Self shows wherein the first interconnection controller includes a reinitialization indicator configurable to direct the first interconnection controller to reinitialize the link (column 8, lines 28-38; column 9, lines 15-27).

In reference to claims 17 and 28, Self shows wherein reinitialization comprises having a transmitter associated with the first interconnection controller send training sequence to the second interconnection controller (column 8, lines 28-38; column 9, lines 15-27).

In reference to claims 20 and 31, Self shows wherein reinitialization comprises having a associated with the first interconnection controller send an initialization sequence to the second interconnection controller (column 14, lines 10-26).

In reference to claim 21, Self shows wherein the first interconnection controller includes a plurality of cluster ID indicators operable to hold values identifying remote clusters of processors (column 14, lines 11-26).

In reference to claim 22, Self shows wherein the first interconnection controller includes, fence, reinitialization and cluster ID bits (column 11, lines 46-column 12, line 8; column

11, lines 46-column 12, line 8) and Booth shows configuration space registers comprising physical layer enable (column 13, lines 63-column 14, line 8).

Claims 3, and 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Self in view of Barroso, as applied to claim 1 above, and further in view of Booth (US Patent 6,065,073), hereinafter referred to as Self, Barroso and Both respectively.

In reference to claim 3, Self and Barroso fail to teach the computer system wherein the first interconnection controller includes a physical layer enable indicator. Nonetheless, this would have been an obvious modification to the system for one of ordinary skill in the art at the time of the invention, as further evidenced by Booth.

In an analogous art, Booth discloses polling for network links (abstract). Booth further shows wherein the first interconnection controller includes a physical layer enable indicator (column 13, lines 63-column 14, line 8). One of ordinary skill in the art at the time of the invention, would be motivated to according modify the system of Self and Barroso so as to provide link monitoring for establishing communication links on the physical layer, while advantageously freeing up CPU bandwidth (i.e. disabling), (Booth; column 6, lines 30-40).

In reference to claim 7, Booth shows wherein the transmitter sends the training sequence when the polling active state is set (column 20, line 55-column 21, line 6).

In reference to claim 8, Booth shows wherein the transmitter does not sent the training sequence when the polling sleep state is set (column 20, line 55-column 21, line 6).

Claims 13-14, 18-19, 24-25 and 29-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Self in view Barroso and Sgroi, as applied to claims 12 and 23 above, and further in view of Booth (US Patent 6,065,073), hereinafter referred to as Self, Barroso, Sgroi and Booth respectively.

In reference to claims 13 and 24 Self, Barroso and Sgroi fail to disclose the method wherein polling is performed continuously. Nonetheless, this would have been an obvious modification to the method for one of ordinary skill in the art at the time of the invention, as further evidenced by Booth.

In an analogous art, Booth discloses polling for network link (abstract). Booth further discloses wherein polling is performed continuously (column 20, line 55-column 21, line 6). One of ordinary skill in the art at the time of the invention would be motivated to according modify the system of Self , Barroso and Sgroi with polling so as to provide link monitoring for establishing communication links, while advantageously freeing up CPU bandwidth (i.e. disabling), (Booth; column 6, lines 30-40).

In reference to claims 14 and 25, Booth shows wherein the first interconnection controller includes a physical layer enable indicator (column 13, lines 63-column 14, line 8).

In reference to claims 18 and 29, Booth shows wherein the transmitter sends the training sequence when the polling active state is set (column 20, line 55-column 21, line 6).

In reference to claims 19 and 30, Booth shows wherein the transmitter does not sent the training sequence when the polling sleep state is set (column 20, line 55-column 21, line 6).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LASHANYA R. NASH whose telephone number is (571)272-3957. The examiner can normally be reached on 9am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ario Etienne can be reached on (571) 272-4001. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/LaShanya R Nash/
Examiner, Art Unit 2453
October 22, 2008

/ARIO ETIENNE/
Supervisory Patent Examiner, Art Unit 2457